electrically connecting a plurality of contact pads on a surface of a semiconductor chip to corresponding bond pads on a circuitized substrate such that the connections create a gap between the chip and the substrate, wherein the substrate is rigid;

sealing the gap between the chip and the substrate with a fluid, curable encapsulant so that there is a void therebetween;

applying pressure to the assembly causing the encapsulant to flow into the gap and around the connections; and

applying energy to the assembly in order to cure the encapsulant.

2. The method as claimed in claim 1, wherein the pressure applying step is conducted for a time period that is between 30 minutes to several hours.

3. The method as claimed in claim 1, wherein the pressure applying includes gradually increasing the applied pressure.

4. A method of injecting an encapsulant between a face surface of a semiconductor chip and a juxtaposed substrate, comprising:

providing a gap between the face surface of the chip and the substrate, wherein the substrate is rigid;

sealing each edge of the gap with a curable fluid encapsulant so that there is a void between the chip and the substrate;

applying pressure to cause the encapsulant to flow between the chip and the substrate; and

applying energy to cure the encapsulant.

5/6. The method as claimed in claim 4/5, wherein the pressure applying step is conducted for a time period that is between 30 minutes to several hours.

6/7. The method as claimed in claim 4/5, wherein the pressure applying includes gradually increasing the applied pressure.

7/8. The method as claimed in claim 4/5, wherein the applied pressure is between about 10 and 450 pounds per square inch.

8/9. The method as claimed in claim 4/5, wherein the applied pressure is between about 30 and 200 pounds per square inch.

9/10. The method as claimed in claim 4/5, wherein the gap providing step includes:

providing compliant pads on the substrate, wherein each of the compliant pads includes a peelable tacky surface to which the face surface of the chip is releasably attached.

11. A method of treating an interposer layer for a semiconductor package assembly to provide a substantially void free interposer layer, comprising:

disposing a sheet-like, compliant interposer layer between a face surface of a semiconductor chip and a surface of a substrate such that voids within or at the boundaries of the interposer layer are sealed within the assembly, wherein the substrate is rigid; and

applying pressure to the assembly wherein the voids in the interposer layer are substantially eliminated.

12. The method as claimed in claim 11, wherein the pressure applying step is conducted for a time period that is at least one hour.

13. The method as claimed in claim 11, wherein the pressure applying includes gradually increasing the applied pressure.

14. The method as claimed in claim 11, wherein the applied pressure is between about 10 and 1000 pounds per square inch.

15. A method of creating a void-free interposer layer for a microelectronic component, comprising:

injecting an interposer layer into a gap between a microelectronic component and a sheet-like substrate such that voids within or at the boundaries of the interposer are sealed within the gap, wherein the substrate is rigid; and

applying pressure wherein the voids in the interposer layer are substantially eliminated.

16. The method as claimed in claim 15, wherein the pressure applying step is conducted for a time period that is at least one hour.

17. The method as claimed in claim 15, wherein the pressure applying includes gradually increasing the applied pressure.

18. The method as claimed in claim 16, wherein the applied pressure is between about 10 and 1000 pounds per square inch.

19. The method as claimed in claim 16, wherein the microelectronic device is a semiconductor chip.

20. The method as claimed in claim 16, wherein the microelectronic device is a heat spreader.

21. The method as claimed in claim 16, wherein the microelectronic device is comprised of a support ring encircling a semiconductor chip.

22. A method of providing a substantially void free underfill for a semiconductor wafer having a plurality of flip chip assemblies, comprising:

electrically connecting a plurality of contact pads of flip chip assemblies disposed on a surface of a semiconductor wafer to corresponding bond pads on a circuitized substrate such that the connections create a gap between the flip chip assemblies and the substrate, wherein the substrate is rigid;

A1 contd

sealing the gap between the flip chip assemblies and the substrate with a fluid, curable encapsulant so that there is a void therebetween;

applying pressure to cause the encapsulant to flow into the gap and around the connections; and

applying energy to cure the encapsulant.

11 ~~23~~. The method as claimed in claim 10 ~~22~~, wherein the pressure applying step is conducted for a time period that is between 30 minutes to several hours.

12 ~~24~~. The method as claimed in claim 10 ~~22~~, wherein the pressure applying includes gradually increasing the applied pressure.

13 ~~25~~. A method of injecting an encapsulant between a face surface of a semiconductor wafer and a juxtaposed substrate, comprising:

providing a gap between the face surface of the wafer and the substrate, wherein the substrate is rigid;

sealing each edge of the gap with a curable fluid encapsulant so that there is a void between the wafer and the substrate;

applying pressure to cause the encapsulant to flow between the wafer and the substrate; and

applying energy to cure the encapsulant.

A1 cont'd

14 ~~28~~. The method as claimed in claim 13 ~~25~~, wherein the pressure applying step is conducted for a time period that is between 30 minutes to several hours.

15 ~~27~~. The method as claimed in claim 13 ~~25~~, wherein the pressure applying includes gradually increasing the applied pressure.

16 ~~28~~. The method as claimed in claim 13 ~~25~~, wherein the applied pressure is between about 10 and 450 pounds per square inch.

17 ~~29~~. The method as claimed in claim 13 ~~25~~, wherein the applied pressure is between about 30 and 200 pounds per square inch.

18 ~~30~~. The method as claimed in claim 13 ~~25~~, wherein the gap providing step includes:

providing compliant pads on the substrate so as to provide the gap between the face surface of the wafer and the substrate, wherein each of the compliant pads includes a peelable tacky surface to which the face surface of the wafer is releasably attached.

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